REMARKS

This amendment is in response to the Office Action having a mailing date of July 10, 2003, the deadline to which has been extended by one (1) month from October 10, 2003 to November 10, 2003, by petition and payment of fee.

Claims 1-13 are pending in the present Application. Claims 1-12 have been rejected. Claim 13 has been allowed. Claims 4 and 10-12 have been amended for clarification and to correct grammatical and typographical errors. Claims 1-3, 5, 6, 8 and 9 have been cancelled. Accordingly, claims 4 and 10-13 remain pending in the present application.

In the Specification

Applicant has amended the specification under "CROSS-RELATED APPLICATIONS" to list the specific serial numbers for all seven applications related to the present application.

Allowed Claim

Applicant appreciates and acknowledges allowance of claim 13.

35 U.S.C. §102 Rejections

The Examiner has stated:

> **Claims 1-3, 4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Calvignac et al. (US2002/0122386 A1).**
>
> **As to claim 1, Calvignac et al. disclose high speed network processor comprising a plurality of standard cells (for example data storage memory); at least one field programmable gate array (FPGA) cell (Fig. 1, FPGA) that can communicate with at least one of standard cells, wherein the FPGA cell allows for customization of the network processor (FPGA is programmable) (Figs. 1-4)**
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> **As to claim 2-3, 4 and 7, remarks set forth in claim 1 equally apply here in r j cting claims 4 and 7. In addition, Calvignac et al. t ach wh rein the at least one FPGA cell can**

provide a specific function based upon fi ld pr gramming techniqu s t allow f r cust mizati n of th network processor (FPGA is pr grammable devic); wherein th standard c lls ar utiliz d f r comm n l gic and th at l ast one FPGA cell is utiliz d for high risk l gic (FPGA is programmabl).

Claims 1-12 are r ject d under 35 U.S.C. 102(a) as b ing anticipat d by Pr duct R vi w fr m Adaptiv Silicon Inc. (ASi), "Adaptive Silic n Ann unces FPGA Cor , March 12, 2001, pages 1-4.

As to claims 1-8, ASi discloses a customizable network processor comprising embedded programmable logic core within ASIC and ASSP in a single silicon die. The first embedded programmable logic core will enable ASIC and ASSP manufacturers to add the flexibility and reduce the engineering costs of FPGAs to their products said CEO of ASi. The embedded programmable logic core permits the high-risk blocks (high-risk logic) of an SoC device to be modified after first silicon is produced. Consequently, such devices may be fabricated earlier in the development process without risking modification to the overall design or re-spinning the silicon. The embedded programmable logic core also provides the flexibility to modify devices once they are shipped to customers. As a result, algorithms can be upgraded and changes in standards or protocols can be accommodated in applications like communications and image processing. By architecting a family of products with embedded programmable logic, it is possible to produce a number of different silicon products from single die, avoiding the increasing costs of masks, prototype silicon and parallel engineering development efforts. For design like networking products and wireless base station applications, which are marked by evolving standards, embedded programmable logic allows the design to be completed and the silicon built while changes are being made. Changes are possible right up until product is finally released to customers. For applications like network processor chip, where custom processsors are often implemented, co-processor or instruction-level functions can be implemented to complement the primary processor functions. Thus, ASi introduces a network processor comprising hybrid of FPGAs and ASICs or in standard products. It is noted that custom logic file including a verification module to verify customized network processor, and custom logic bill are inherently within a customable network processor introduced by ASi comprising embedded programmable logic (FPGA) that permits high-risk blocks (high-risk logic) on an SoC device to be modified after first silicon is produced or in the process to produce. Since changes are possible right up until the product (customized network processor) is finally released to customers, the network processor is verified accordingly based on custom logic file or custom request.

As to claims 9-12, since ASi introduces a customized network processor, said customized network processor inherently includes a processor local bus (PLB), two on-chip peripheral buses (OPBs), an accelerator function and a PLB master/slave function for internal and external communications and in order to customize network processor according to customer need.

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Craig Matsumoto, "Lucent hybrid combines FPGA, ASIC features," EE times, August 18, 2000, page 1.

As to claims 1-12, Matsumoto describes that Lucent discloses hybrid FPGA and standard-cell ASIC features for a networking communications application including a network processor. Since FPGA is programmable, thus the FPGA cell allows for customizati n for th n twork proc ssor. Matsumot describes that pr grammable logic is added to the chips including FPGAs and ASICs. Since FPGAs are programmabl , the FPGAs pr vid a sp cific function bas d upon field programming techniques to allow for customization of the network proc ss r, and the plurality f standard cells ar utilized f r

comm n logic and th at least n FPGA cell is utilized for high risk l gic becaus th added FPGA would cust mize th network processor acc rding to customer need. Accordingly, a custom l gic file including a verificati n modul is inherently included within hybrid f FPGAs and standard-cell ASICs f rming a n twork pr cessor, since adding FPGA w uld require v rification in ord r to m et d sign requir ments. It is not d that a proc ssor l cal bus (PLB), tw on-chip peripheral buses (OPBs), an accelerator functi n and a PLB master/slav functi n are inher ntly includ d within th hybrid FPGAs and standard-c ll ASICs of a network processor chip.

Claims 1-12 are rejected under 35 U.S.C. 102(a) as being anticipated by Mason et al. (6,272,451).

As to claims 1-12, Mason et al. teach a field-programmable-system-level integrated circuit (FPSLIC) that can be used as a network processor (Figs. 1A-1B), col. 1, summary, col. 5, line 65 to col. 12, line 25) comprising a plurality of standard cells (standard-cell ASIC and ASSP, col. 6); a plurality of FPGAs cells, wherein the FPGAs allow customization of the network processor. The network processor comprising FPSLIC architecture is ideal for implementation of networking, telecommunications, multimedia, audio, handled, portable, and industrial control applications (col. 6). Thus, the FPGAs allow for customization of the network processor to be suitable for such above applications. Accordingly, the standard-cell ASIC and ASSP are utilized for common logic and at one of the FPGAs is utilized for high risk logic, since FPGAs can be embedded in FPSLIC chip designed to be suitable for an application. Since, the FPGA core is embedded within FPSLIC chip that can be used for an application (customer need), the FPSLIC is designed by providing a custom logic file with a verification module in order to verify a complete FPSLIC design or a complete network processor. Since, the FPSLIC chip (network processor) is designed for these above applications, said FPSLIC chip would comprise a processor local bus (PLB), two on-chip peripheral buses (OPBs), an accelerator function and a PLB master/slave function (col. 5-col. 11).

Applicants respectfully traverse this rejection. Claim 7 has been amended to clarify the present invention by using similar language to that recited in claim 13. Claim 7 recites a network processor which includes elements which are not disclosed in combination in any of the cited references, namely, none of the references teach or suggest a network processor comprising a plurality of standard cells. The plurality of standard cells comprising common logic. The network processor including a plurality of FPGA cells. The plurality of FPGA cells comprising high risk logic. The network processor further including a first bus and two peripheral busses coupled to a portion of the standard cells and portion of the FPGA cells. The FPGA cells coupled to the first comprise a first function and second functions. The FPGA cells coupled to one of the two peripheral busses are interfaces. The FPGA cells coupled to the other of the two peripheral busses are a third and a fourth function. The plurality of cells each can provide a

specified function based upon field programming techniques to allow for customization of the network processor.

Dependent claims 10-12 are allowable and they depend from an allowable base claim.

Claim 4

None of the cited references teach or suggest a method for customizing a network processor where a custom logic file which includes a verification module is provided to the vendor by a customer and wherein the customer provided verification module is utilized to verify the customized network processor.

Conclusion

In view of the foregoing, Applicants submit that claims 1-12 are patentable over the cited references. Applicants, therefore, respectfully request reconsideration and allowance of the claims as now presented.

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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Date

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